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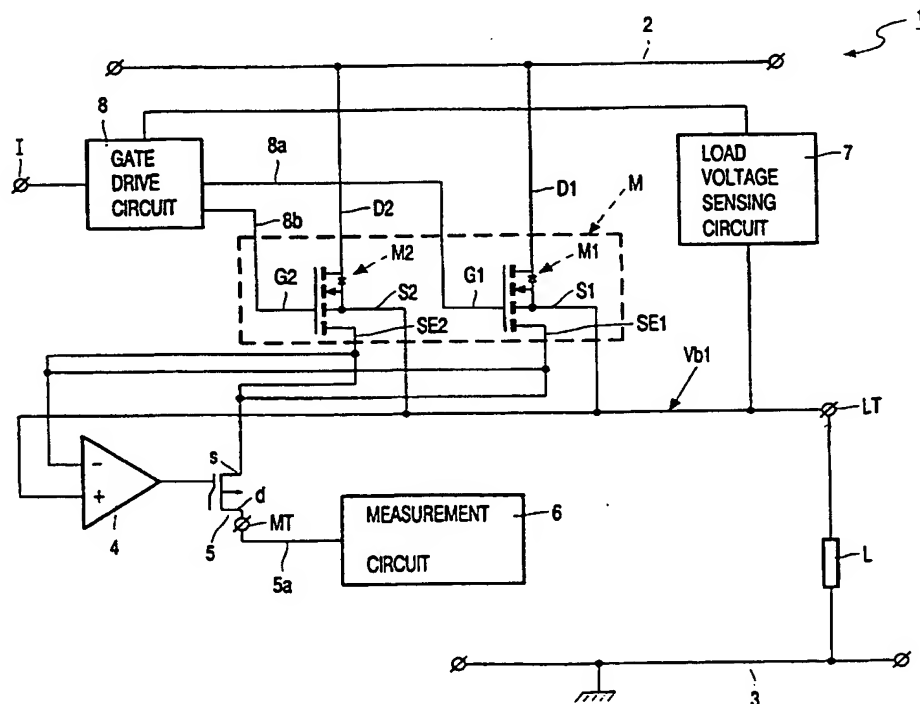
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(54) Title: A POWER SWITCHING CIRCUIT

**(57) Abstract**

A power switching circuit has: first and second voltage supply lines (2 and 3); a control signal input terminal (I); a load terminal (LT); and a measurement terminal (MT). A power semiconductor switch (M) has a main current carrying section (MC1 and MC2) and a sense current carrying section (SC1 and SC2) for carrying a current which is proportional to and smaller than the current carried by the main current carrying section. The main current carrying section is formed of a plurality of subsidiary current carrying sections (MC1 and MC2). Each subsidiary current carrying section has a subsidiary main current carrying electrode (S1 and S2) coupled to the load terminal (LT) so that the subsidiary electrodes together form the main current carrying electrode. Each subsidiary main current

carrying section has a respective different control electrode (G1 and G2). A control circuit (7) is provided for sensing the voltage at the load terminal (LT) and for separately controlling the supply of a control signal from the control signal input terminal (I) to each of the control electrodes (G1 and G2) in dependence upon the sensed voltage.



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## DESCRIPTION

## A POWER SWITCHING CIRCUIT

This invention relates to a power switching circuit having a power semiconductor switch, which circuit has particular, but not exclusive, application in the automotive industry.

The power semiconductor switch of such a power switching circuit comprises a plurality of parallel-connected active cells, source cells where the power semiconductor switch is a power MOSFET or an insulated gate bipolar transistor (IGBT).

As disclosed in, for example, EP-A-0 139 998 it is known to separate the active cells into a main current carrying section containing the majority of the active cells and a sense or emulation current carrying section containing only a few of the active cells by, in the case of a power MOSFET or IGBT, providing separate connections to the sources of the active cells of the main current carrying section and of the sense current carrying section. As disclosed in EP-A-0 139 998, the current flowing through the main current carrying section should be related to that flowing through the sense current carrying section by a constant  $K$  given by the ratio of the active areas of the main current carrying and sense current carrying sections, that is the ratio between the number of active cells in these two sections when all the active cells are identical. Therefore sensing the current flowing through the current carrying section should enable a determination to be made as to the current flowing through the main current carrying section of the device. This enables, for example, detection of faults in the power semiconductor switch itself or the detection of, for example, a short or open circuit when the load which the power switch is arranged to switch is defective.

However, under certain circumstances, for example change in the input impedance of the circuit used to sense the current flowing through the sense current carrying section or in the input impedance of the load connected to the semiconductor power switch, the current flowing through the sense current

carrying section may not be proportional to that flowing through the main current carrying section. US-A-5081379 addresses this problem by providing a voltage impression device which impresses the voltage of the source electrode (in the case of a power MOSFET or IGBT) of the main current carrying section on the source electrode of the sense current carrying section.

As disclosed in US-A-5081379, the voltage impression device comprises a differential amplifier having its non-inverting input connected to the source electrode of the main current carrying section and its inverting input connected to the source electrode of the sense current carrying section. The output of the differential amplifier is connected to the control electrode of control transistor (a p-channel IGFET (insulated gate field effect transistor) in the example given where the power switch is an n-channel power MOSFET)) having its source electrode connected to the source electrode of the sense current carrying section of the power semiconductor switch.

Even in the power switching circuit disclosed in US-A-5081379 the current flowing through the main current carrying section is not exactly related to measured current by the factor  $K$ , rather the current through the main current carrying section is related to the measured current by:

$$K \cdot (1 - V_{\text{off}}/V_{\text{bl}})$$

where  $V_{\text{off}}$  is the input offset voltage of the differential amplifier and  $V_{\text{bl}}$  is the voltage at the load with respect to the positive supply voltage where the power semiconductor switch is a high side switch for connecting a load to a positive voltage supply line (such as the positive terminal of the battery where the power switching circuit is used in an automotive application).

At high current levels  $V_{\text{bl}}$  is significantly bigger than  $V_{\text{off}}$  and so the error,  $V_{\text{off}}/V_{\text{bl}}$ , in the measure of the current through the load obtained by sensing the current through the sense current carrying section is small. However, at low current levels, the amplifier input offset voltage  $V_{\text{off}}$  presents a significant part of the load voltage and gives rise to a significant error. Previously, this problem has been addressed by increasing the load voltage by reducing the voltage applied to the control electrode of the power semiconductor switch relative to the load voltage  $V_{\text{bl}}$ , thereby increasing the on-resistance of the power switch. The

problem with this approach is that reducing the drive voltage to the control electrode in order to increase the on-resistance of the power semiconductor switch takes the power switch out of its linear operation region so that the relationship between the sensed current and that flowing through the main current carrying section becomes dependent on the difference between the control electrode and offset voltage squared resulting in the current through the main current carrying sections being related to the measured current by:

$$K \cdot (V_{gs} - V_t - V_{off})^2 / (V_{gs} - V_t)^2$$

where  $V_t$  is the threshold voltage of the power switch and  $V_{gs}$  is the voltage between the control and source electrodes of the main and sense current carrying sections. As can be seen from a comparison of equations 1 and 2, this approach results in the offset voltage having an even more significant effect giving rise to an even greater error as the sense error has terms proportional to  $V_{off}$  and  $V_{off}$  squared.

Such problems may be reduced, but not eliminated, by using a high precision operational amplifier with an extremely low offset voltage. This would, however, significantly increase the cost of the power switching circuit.

It is an aim of the present invention to provide a power switching circuit which enables errors in the measure of the current through the main current carrying section arising from the voltage offset of the amplifier to be avoided or at least reduced without the necessity for using an extremely high precision operational amplifier.

In one aspect, the present invention provides a power switching circuit comprising a power semiconductor switch, which may be intended to operate as a high-side switch, having a main current carrying section and a sense current carrying section for carrying a smaller current than the main current carrying section, the first and second current carrying sections sharing a common first main electrode, the main current carrying section having a main current carrying electrode for connection to a load and the sense current carrying section having a sense current carrying electrode for enabling the current through the sense current carrying section to be measured, wherein at least the main current

carrying section is formed of a plurality of subsidiary current carrying sections, means are provided for sensing the voltage at the main current carrying electrode and for switching off or reducing the current through at least one of the plurality of subsidiary current carrying sections of the main current carrying section when the voltage at the main current carrying electrode drops below a  
5 predetermined value so as thereby to increase the resistance through the power semiconductor switch device while maintaining the power semiconductor switch in its linear operation region.

According to one aspect of the present invention, there is provided a  
10 power switching circuit as set out in claim 1.

This enables accurate measurement of the current flow through the power semiconductor switch at low current levels by increasing the on-resistance in a manner which allows the power semiconductor switch device to remain in its linear operation region.

15 Various preferred features in accordance with the invention are set out in claims 1 to 15.

These and other advantageous features in accordance with the invention will now be illustrated in embodiments of the present invention, now to be  
20 described with reference to the accompanying drawings, in which:

Figure 1 shows a partly block-schematic circuit diagram of a first embodiment of a power switching circuit in accordance with the present invention;

Figure 2 shows a partly block-schematic circuit diagram of a second  
25 embodiment of a power switching circuit in accordance with the present invention;

Figure 3 shows an example of a measurement circuit suitable for use in the power switching circuit shown in Figure 1 or Figure 2;

Figure 4 is a graph showing the load terminal voltage ( $V_{bl}$ ) in volts of the  
30 circuit shown in Figure 1 or 2 against the load current ( $I_L$ );

Figure 5 shows a top plan view of part of a power semiconductor switch for use in the circuit shown in Figure 1 or 2 with certain surface layers omitted for illustrative purposes;

Figures 6 and 7 show cross-sectional views taken along lines VI-VI and VII-VII, respectively, in Figure 5; and

Figure 8 shows a fragmentary cross-sectional view, similar to that shown in Figures 6 and 7, through part of a semiconductor body to show the structure of logic transistors integrated with the power semiconductor switch shown in Figures 5 to 7.

It should be noted that the figures are diagrammatic and are not drawn to scale. In particular, in Figures 6 to 8, relative dimensions and proportions of parts of the drawings have been shown exaggerated or reduced in size, for the sake of clarity and convenience in the drawings. The same reference signs are generally used to refer to corresponding or similar features throughout the drawings.

Figure 1 shows a part block-schematic circuit diagram of a first embodiment of a power switching circuit 1 in accordance with the present invention.

The power switching circuit 1 comprises a power semiconductor switch in the form of an n-channel enhancement mode power vertical MOSFET having, as is known in the art, many tens of thousands of parallel-connected source cells sharing a common drain region. The power MOSFET M is arranged to be coupled as a high-side switch that is with its drain electrode D1, D2 coupled to a positive voltage supply line 2 and its source electrode S1, S2 (collectively referred to as "S" herein) coupled to a load terminal LT to which a load L is connectable so as to connect the load between an earth or ground voltage supply line 3 and the positive voltage supply line 2 via the power MOSFET M. The gate or control electrode G1, G2 of the power MOSFET M is coupled to a control input line I via a gate drive circuit 8.

As is known from, for example, EP-A-0 139 998, the power switching device is separated into a main current carrying section and a sense current

carrying section by patterning the source metallisation so that a number of the source cells are isolated from the main source electrode S1, S2 and connected to a separate sensing electrode SE1, SE2 (collectively referred to as "SE" herein).

5           Theoretically, the current through the main current carrying section should be related to the current through the sense current carrying section multiplied by the ratio of the number of source cells in the main current carrying section divided by the number of source cells in the sense current carrying section. This, however, is only the case if the voltages at the source S and sense SE  
10   electrodes are the same. In order to achieve this, as disclosed in US-A-5081379 discussed above, a voltage impression device is used to impress the voltage at the source electrode S onto the sense electrode SE. As shown in Figure 1, the voltage impression device comprises a differential amplifier 4 having its inverting input connected to the sense electrode SE and its non-inverting input connected  
15   to the source electrode S. The output of the differential amplifier 4 is connected to the control electrode of a control transistor 5 of the voltage impression device. In the example shown, the control transistor 5 is a p-channel enhancement mode insulated gate field effect transistor having its source electrode connected to the sense electrode SE and its drain electrode connected at a measurement  
20   terminal MT to a measurement circuit 6 for measuring the current flowing through the sense electrode. The differential amplifier 4 and the control transistor 5 may be integrated into the same semiconductor body as the power semiconductor switch M as will be detailed below.

25           To facilitate differentiation, power insulated gate field effect transistors are referred to herein as MOSFETs while logic insulated gate field effect transistors are referred to herein as IGFETs.

30           As described so far, the power switching circuit 1 shown in Figure 1 is the same as that disclosed in US-A-5081379 with the voltage impression device 4, 5 serving to impress the source electrode voltage onto the sense electrode voltage so that the current through the sense current carrying section represents a proportion of the current flowing through the main current carrying section.



In contrast to the arrangement shown in US-A-5081379, the main current carrying section and the sense current carrying section of the power semiconductor switch M shown in Figure 1 are split into a number of subsidiary sections as will be described below. In the arrangement shown in Figure 1, the power semiconductor switch M has two subsidiary main current carrying sections each having a corresponding sense current carrying section and is illustrated schematically as two parallel-connected MOSFETs M1 and M2 with the drain electrodes D1 and D2 of the two MOSFETs M1 and M2 connected to the power supply line 2, the source electrodes S1 and S2 connected to the load terminal LT and to the non-inverting input of the differential amplifier 4 and the two sense electrodes SE1 and SE2 connected to the inverting input of the differential amplifier 4 and also to the source electrode of the p-channel IGFET 5. As shown in Figure 1, separate gate or control electrodes G1 and G2 are provided for the MOSFETs M1 and M2.

A load voltage sensing circuit 7 is provided to sense the voltage  $V_{bl}$  at the load terminal LT with respect to the positive supply voltage, that is the voltage across the power switch (i.e. the voltage at the source electrodes S1 and S2). The load voltage sensing circuit 7 controls the gate drive circuit 8 which has first and second outputs 8a and 8b connected to the control electrodes G1 and G2, respectively.

As set out above, the ratio between the measured current and the current through the main current carrying section is given by:

$$K \cdot (1 - V_{off} / V_{bl})$$

where  $V_{off}$  is the input offset voltage of the differential amplifier 4,  $V_{bl}$  is the load voltage and  $K$  is the geometric area ratio of the sense to main current carrying sections which, because the source cells are all of the same size, is given by the ratio of the number of these source cells.

In operation of the circuit shown in Figure 1, when the load voltage sensing circuit 7 determines that the load voltage  $V_{bl}$  has become so low that the input offset voltage  $V_{off}$  of the differential amplifier 4 has a significant affect on the measure of the current ratio, then the load voltage sensing circuit 7 causes the gate drive circuit 8 to switch off or reduce the gate drive voltage to one of the

control electrodes G1 and G2 of the power semiconductor switch M so as to leave only one of the MOSFETs M1 and M2 conducting. As will be appreciated by the person skilled in the art, because a MOSFET with a smaller number of source cells is now conducting, this will increase the on-resistance of the power semiconductor switch so raising the voltage  $V_{bl}$  at the load terminal LT, and thereby reducing the effect of the offset voltage of the differential amplifier 4 on the measure of the current ratio, while still allowing the power semiconductor switch M to operate in its linear region.

Typically, the load voltage sensing circuit 7 may be arranged to cause the gate drive circuit 8 to switch off or reduce the drive voltage to one of the MOSFETs M1 and M2 when the voltage at the load terminal LT is of the order of only about ten times the input offset voltage  $V_{off}$  of the differential amplifier 4.

Figure 2 shows another embodiment of a power switching circuit in accordance with the invention. The power semiconductor switch M, differential amplifier 4, control transistor 5 and measurement circuit 6 shown in Figure 2 are the same as the equivalent components shown in Figure 1 and will not be described again.

In the circuit shown in Figure 2, the input control signal line I is coupled via a charge pump driver 81 and line 81a to the control gate G1 and via a charge pump driver 82 and line 82a to the control gate G2. The charge pump drivers may be of any known form and, as will be understood by the person skilled in the art, enable sufficient voltage to turn on the MOSFETs M1 and M2 to be derived from the signal on the input signal control line I. The gate drive circuit 8 also comprises two n-channel enhancement mode IGFETs N1 and N2 each having their control gate G1 and G2 coupled to the input control signal line I via an inverter 83 and line 83a so that the IGFETs N1 and N2 are rendered conducting when the signal on the input signal control line I is low and vice versa.

The source electrode s1 of IGFET N1 is coupled to the source electrode S1 of the power semiconductor switch M while the source electrode s1 of the IGFET N2 is coupled to the source electrode S2 of the power semiconductor switch M. The drain electrode d1 of the IGFET N1 is coupled to the control gate G2 while the drain electrode d2 of the IGFET N2 is coupled to the control gate G1 of the

power semiconductor switch M. The IGFETs N1 and N2 form control transistors for removing the gate drive from the control gates G1 and G2 and thus turning off the power semiconductor switch M when a turn-off signal is applied to the control input line I.

5 As shown in Figure 2, the load voltage sensing circuit 7 comprises a comparator 70 and a third n-channel enhancement mode IGFET N3 having its drain electrode d3 coupled to one of the control gates G1 and G2 of the power semiconductor switch M1, in this case coupled to the control gate G1. The source electrode s3 of the third IGFET N3 is coupled to the source electrodes S1  
10 and S2 of the power semiconductor switch M1. The sense electrodes SE1 and SE2 of the power semiconductor switch M are coupled to the inverting input of the comparator 70 which has its non-inverting input coupled to a reference voltage Vref and its output coupled to the control gate g3 of the third IGFET N3.

In operation of the circuit shown in Figure 2, when the voltage at the load  
15 terminal LT and thus the voltage at the sense electrodes SE1 and SE2 falls to Vref, the output of the comparator 70 goes high turning on the third n-channel IGFET N3 and so pulling down the control gate G1 thereby rendering the power MOSFET M1 non-conducting and so reducing the number of source cells and thus increasing the on-resistance of the power semiconductor switch M.  
20 Typically, the on-resistance of the power semiconductor switch M will be 30m Ohm (milliohms) when both MOSFETs M1 and M2 are conducting and 300m Ohm when only MOSFET M2 is conducting.

Where the offset voltage of the comparator 70 is 5 millivolts (mV), then Vref will generally be 50 millivolts. Any known reference voltage source may be  
25 used, for example a bandgap reference voltage source may be used.

The use of the comparator 70 shown in Figure 2 provides for a sharp abrupt transition in the on-resistance of the power semiconductor switch M. This is illustrated by the solid line A in the graph of load voltage Vbl (in volts) against current IL (in amps) shown in Figure 4. As can be seen from Figure 4, when the  
30 load voltage Vbl falls to the reference voltage Vref, the third IGFET N3 is rendered conducting so switching off the power MOSFET M1, immediately increasing the on-resistance of the power semiconductor switch M and thus

causing a rapid increase in the load voltage  $V_{bl}$  bringing the load voltage up to point A1 in Figure 4 for the same load current  $I_L$ . The comparator 70 is provided with hysteresis in known manner so that, as can be seen from Figure 4, the power MOSFET M1 is not rendered conducting again until the load voltage  $V_{bl}$  reaches V1 which is, in this embodiment, at least 450mV (millivolts) greater than  $V_{ref}$ . In this example V1 is 600mV greater than  $V_{ref}$ .

The comparator 70 shown in Figure 2 may be replaced by an operational amplifier which, as indicated by the dashed line B in Figure 4, does not immediately pull down the gate G1 of the power MOSFET M1 so as to switch that MOSFET off when the reference voltage  $V_{ref}$  is reached, but rather gradually renders the IGFET N3 conducting and so gradually reduces the drive to the gate G1 so as to switch the power MOSFET M1 off gradually. This has the advantage of providing a smooth switch over transition with no step in the load voltage. This use of a comparator does, however, have the advantage that comparators generally require less semiconductor area than operational amplifiers.

The measurement circuit shown in Figures 1 and 2 may be any suitable known measurement circuit. Figure 3 shows block schematically an example of a typical measurement circuit. In the circuit shown in Figure 3, the measurement terminal MT is coupled by a line 5a to a high resistance resistor R1 which is itself coupled to the earth or ground voltage supply line 3. The junction J1 is coupled to an analogue-to-digital (A/D) converter 30 that converts the analogue voltage at junction J1 into a digital signal which is then supplied to a microcontroller 31 which monitors the load current and supplies an output signal that may be used in known manner to, for example, control operation of the power switch or to supply an error or alarm signal. As another example, a current level detection circuit may be used as disclosed in US-A-5081379.

The power semiconductor switch M is, as described above, an n-channel enhancement mode MOSFET. Figures 5 to 7 illustrate the MOSFET M in more detail. In particular, Figures 6 and 7 are cross-sectional views through part of the power semiconductor switch M while Figure 5 shows a top plan view looking in

the direction of arrow C in Figures 6 and 7 but with the top metallisation (source and gate metallisation) omitted.

As shown in Figures 6 and 7, the power semiconductor switch M comprises a monocrystalline silicon semiconductor body 100 having first and second opposed major surfaces 101 and 102. A trench 103 extends into the first major surface 101 so as to define at the first major surface a regular array of polygonal source cells 104 (Figure 5) each bounded by the trench 103 as shown in Figure 5. Typically the device will consist of many tens of thousands of identical source cells.

Each polygonal source cell 104 contains a source region 105 of one conductivity type, in this example n-conductivity type, and a body region 106 of the opposite conductivity type, in this example p-conductivity type, with the body region 106 separating the source regions 105 from a common further region 100a of the one conductivity type so as to define a respective conduction channel area or channel accommodating portion 106a extending between each source region 105 and the common further region 100a. Each polygonal source cell 104 may contain, as shown in Figures 6 and 7, a central region 160b of the same conductivity type as the body region 106 but more highly doped so as to move the point of avalanche breakdown away from the corners of the trench and so as to control the hole current conduction path through the power MOSFET, thereby improving the ruggedness of the power MOSFET.

A drain electrode 108 makes ohmic contact to a more highly doped region 100b of the one conductivity type upon which the common further region 100a is formed. The common further region 100a thus forms the drain drift region and the highly doped region 100b the drain region of the power semiconductor switch M.

A gate dielectric layer 109 in the trench 103 separates a gate conductive layer 110, which may be formed of doped polycrystalline silicon, from the semiconductor body so as to form an insulated gate structure. Insulating regions 112, generally of silicon dioxide, are formed over the gate structure 109, 110 to enable isolation from subsequent source metallisation 113. By patterning of the insulating regions 112 and the metallisation, the same metallisation layer is also

used to enable a gate electrode (not shown in Figures 6 and 7) to make contact to the conductive layer 110 of the insulated gate structure 109, 110.

The power semiconductor switch M is separated into the two MOSFETs M1 and M2 by separating the trench 103 into two isolated trench portions 103a and 103b to provide two separate gates 109, 110 for the MOSFETs M1 and M2. The two MOSFETs M1 and M2 are in turn separated into the main and sense current carrying sections MC1 and MC2 and SC1 and SC2 by patterning of the source metallisation 113 as shown in Figures 5, 6 and 7. The metallisation making contact to the two separate gates 109, 110 is, of course, also patterned to define the two separate gate electrodes G1 and G2. The peripheries of the source and sense metallisation electrodes S1, S2, SE1 and SE2 are shown in Figure 5 so as to illustrate the separation of the power semiconductor switch into the different current carrying sections.

In the embodiments shown in Figures 1 and 2, the MOSFET M1 consists of 50,000 cells while the MOSFET M2 consists of 5,000 cells. The main current carrying section MC1 of the MOSFET M1 has 49,990 source cells (only a few of which are shown in Figure 5) while the sense current carrying section SC1 of the MOSFET M1 has 10 source cells. The MOSFET M2 is smaller with the main and sense current carrying sections MC2 and SC2 having 4,999 (only a few are shown in Figure 5) and one source cell, respectively. It will, of course, be appreciated that the ratio of the number of main current carrying source cells to sense current carrying source cells in each of the MOSFETs M1 and M2 should be the same but the ratio between the number of source cells in the main current carrying sections MC1 and MC2 may be adjusted so as to achieve a particular increase in on-resistance when the MOSFET M1 is switched off as discussed above.

The circuits shown in Figures 1 and 2 use the power semiconductor switch M as a high-side switch, that is the switch M is provided between the positive voltage supply line 2 and the load terminal LT.

In the interest of cost and of compactness, it is desirable for all of the elements (excluding the load L which forms part of the circuit only in use) shown in the circuit of Figure 1 or the circuit of Figure 2 to be integrated into a single

semiconductor chip. As explained in US-A-5081379, especially for automotive applications, the voltage between the power supply lines 2 and 3 may be of the order of 50 to 60 volts. Low power logic transistors N1 to N3 such as IGFETs and the like may be integrated into the same semiconductor body as the power semiconductor switch M by providing complex structural arrangements which isolate the low power logic circuitry from the high side power semiconductor switch M by the provision of special diffusions or barrier layers of differing conductivity types to interpose high breakdown voltage reverse bias pn-junctions between the substrate 100b to which the high voltage is applied and the low power logic devices or by the provision of dielectric isolation. Such expensive, technically complex techniques can, however, be avoided by, as described in US-A-4929884, operating the logic devices with respect to the positive power supply line 2 (that is high side) rather than the earth or ground power supply line 3.

As will be appreciated by those skilled in the art, where the power semiconductor switch M is a high-side switch and is to be used in applications where there is no voltage available above the drain voltage on the voltage supply line 2, then, as shown in Figure 2, the gate drive circuit will, as is known in the art, include charge pumps for enabling the required gate voltages to be achieved at the gates G1 and G2. Such charge pump drivers would, of course, not be necessary if a voltage source sufficient to turn on the power MOSFETs M1 and M2 was available.

Where as described in US-A-4929884, the power switching circuit incorporates high-side logic circuitry, then the gate drive circuit will normally include a level shifter to enable the required gate voltages to be achieved. Again, appropriate level shifters are known in the art.

Figure 8 illustrates part of the semiconductor body 100 showing the structures which may be used to form two different types of n- and p-channel enhancement mode lateral IGFETs in the same semiconductor body 100 as the power semiconductor switch M when the logic is operated from the positive power supply line 2. The first p-channel IGFET Pa shown in Figure 8 has p-conductivity type source and drain regions 200 and 201 formed directly into the

common further region 100a which forms a conduction channel region beneath an insulated gate electrode IG. The first n-channel IGFET Na shown in Figure 8 has a p-conductivity type well 202 within which are formed n-conductivity type source and drain regions 203 and 204 separated by a conduction channel region defined by the p-well 202 and having an insulated gate IG overlying the conduction channel region. The second n- and p-channel IGFETs Nb and Pb shown in Figure 8 differ from the first n- and p-channel IGFETs in that they are designed to be able to withstand higher voltages. To this end, the drain regions 201 and 204 of the second p- and n-channel IGFETs Pb and Nb each have a more lowly doped drain extension region 201a and 204b over which the insulated gate IGa extends. As can be seen from Figure 8, the gate dielectric layer beneath the drain drift regions 201a and 204b is of increased thickness. This structure ensures that the source and conducting channel regions only see low fields because high lateral voltages are dropped across the lowly doped drain extension regions 201a and 204b. The conductive gate CG extends up onto the step in the gate dielectric over the drain extension regions 201a and 204b so as to act as a field plate FP helping to extend the low field beyond the step in the gate dielectric.

As will be appreciated by those skilled in the art, the control transistor 5 shown in Figures 1 and 2 may experience high voltages. Accordingly, this p-channel IGFET (and any other similar p-channels IGFETs) have the structure of the p-channel IGFET Pb shown in Figure 8.

The source cells of the power semiconductor switch shown in Figure 5 are square (with rounded corners) and arranged in a square array. It will, however, be appreciated that other known source cell geometries may be used and that, for example, the source cells may be hexagonal and arranged in a hexagonal close-packed array.

In the embodiments described above, the power semiconductor switch M is a vertical trench MOSFET. However, the power semiconductor switch could also be a power DMOSFET (double diffused MOSFET) as is known in the art and as is illustrated in Figure 2B of US-A-4929884, for example.



The present invention could be applied to applications where the power semiconductor switch is other than a power MOSFET. For example, the power semiconductor switch could be an insulated gate bipolar transistor (IGBT) having the structure shown in Figures 5 to 7 but with the highly doped one conductivity type substrate 100b being replaced by a highly doped substrate of the opposite conductivity type or being formed with highly doped localised regions of the opposite conductivity type extending through the substrate (a so-called anode-shortened IGBT).

In the arrangements described above, the power semiconductor switch is an insulated gate field effect device. However, other field effect power semiconductor devices may be used. For example, the insulated gate may be replaced by so-called Schottky gate technologies in which the gate dielectric layer is omitted and the conductive gate layer forms a Schottky barrier with the lowly doped conduction channel area or accommodating portion. Also, the source regions could be formed as Schottky contact regions rather than diffused regions.

Also, in the embodiments described above, the power semiconductor switch M is a high-side switch. The present invention may, however, also be applied where the power semiconductor switch is a low-side switch. This may be achieved by, for example, effectively inverting the circuit shown in Figure 1 or Figure 2 so that all n-channel devices become p-channel devices and vice versa so that, for example, the n-channel power MOSFET of Figures 1 and 2 would be replaced by p-channel power MOSFET and the p-channel control transistor would be replaced by a n-channel control transistor.

In the embodiments described above, the main and current carrying sections of the power semiconductor switch are each separated into two subsidiary sections. However, the main and sense current carrying sections may each be separated into three or even more subsidiary sections. This may have particular advantage where the load voltage sensing circuit uses a comparator because it would enable the load voltage  $V_{bl}$  to be ramped up in smaller steps. This would, of course, require a separate reference voltage and

comparator for each of the additional main current carrying subsidiary sections so as to control switching in or out of those additional sections.

In the embodiments described above, each main current carrying section of the power semiconductor switch has its own sense current carrying section.

5 However, it may be possible for the main current carrying sections to share a common sense current carrying section. This would, of course, require the measurement circuit to be able to compensate for the change in sense ratio when one of the main current carrying sections was switched off. Also, in the above-described embodiments where each main current carrying section has its  
10 own sense current carrying section, then the ratio of the number of cells in the sense current carrying section to the number of cells in the main current carrying section is the same for each main current carrying section. This need, however, not necessarily be the case although this would make interpretation of the measurement results more complicated.

15 From reading the present disclosure, other variations and modifications will be apparent to a person skilled in the art. Such variations and modifications may involve equivalent and other features which are already known in the design, manufacture and use of semiconductor devices and circuits using such devices and which may be used instead of or in addition to features already  
20 described herein.

Although claims have been formulated in this application to particular combinations of features, it should be understood that the scope of the disclosure of the present invention also includes any novel feature or any novel  
25 combination of features disclosed herein either explicitly or implicitly or any generalisation thereof, whether or not it relates to the same invention as presently claimed in any claim and whether or not it mitigates any or all of the same technical problems as does the present invention.

The applicants hereby give notice that new claims may be formulated to any such features and/or combinations of such features during the prosecution of  
30 the present application or of any further application derived therefrom.

## CLAIMS:

1. A power switching circuit comprising: first and second voltage supply lines; a control signal input terminal; a load terminal for enabling a load to  
5 be coupled between the load terminal and the second voltage supply line; a measurement terminal for coupling to a current measurement circuit; a power semiconductor switch having a main current carrying section and a sense current carrying section for carrying a current which is proportional to and smaller than  
10 the current carried by the main current carrying section, the main and sense current carrying sections having a control electrode coupled to the control input terminal for controlling switching on and off of the power semiconductor switch and a first main electrode coupled to the first voltage supply line, the main current carrying section having a main current carrying electrode coupled to the load  
15 terminal and the sense current carrying section having a sense current carrying main electrode coupled to the measurement terminal, characterised by: at least the main current carrying section comprising a plurality of subsidiary current carrying sections, each subsidiary main current carrying section having a subsidiary main current carrying electrode coupled to the load terminal so that the subsidiary main current carrying electrodes together form the main current  
20 carrying electrode and each subsidiary main current carrying section having a respective different control electrode; and by control means for sensing the voltage at the load terminal and for separately controlling the supply of a control signal from the control signal input to each of the control electrodes in dependence upon the sensed voltage.

25

2. A circuit according to claim 1, wherein the power semiconductor switch is arranged to form a high-side switch with the first voltage supply line being coupled, in use, to a positive voltage and the control means is arranged to control the supply of the input control signal to the control electrodes so as to  
30 switch off one of the subsidiary main current carrying sections when the sensed voltage falls below a predetermined voltage.

3. A circuit according to claim 1 or 2, wherein the different ones of the plurality of main current carrying sections are arranged to carry different currents.

4. A circuit according to claim 1, 2 or 3, wherein the sense current  
5 carrying section comprises a plurality of subsidiary sense current carrying sections with each subsidiary sense current carrying section being associated with and sharing the same control electrode as a corresponding one of the subsidiary main current carrying sections and each subsidiary sense current carrying section having a subsidiary sense current carrying electrode coupled to  
10 the measurement terminal so that the subsidiary sense current carrying electrodes together form the sense current carrying electrode.

5. A circuit according to claim 4, wherein the ratio between the current carrying capabilities of each of said subsidiary main current carrying  
15 sections and the corresponding subsidiary sense current carrying section is the same.

6. A circuit according to any one of the preceding claims, further comprising a voltage impression means for impressing a voltage at the main  
20 current carrying electrode on the sense current carrying electrode.

7. A circuit according to claim 6, wherein the voltage impression means comprises a differential amplifier having an inverting and a non-inverting input and an output with the non-inverting input being coupled to the main current  
25 carrying electrode, the inverting input being coupled to the sense current carrying electrode and the output being coupled to the control electrode of a control transistor having first and second main electrodes coupling the main current path of the control transistor between the sense current carrying electrode and the measurement terminal.

30

8. A circuit according to any one of the preceding claims, wherein the control means comprises an amplifier having an inverting and a non-inverting

and an output with the non-inverting input being coupled to a reference voltage terminal for receiving a reference voltage, the inverting input being coupled to the sense current carrying electrode and the output being coupled to the control electrode of a control transistor having first and second main electrodes coupling the main current path of the control transistor between the control electrode and one of the subsidiary main current carrying electrodes such that, in use, when the voltage at the sense current carrying electrode reaches the reference voltage the control transistor is rendered conducting to reduce or turn off the input control signal to the associated control electrode.

10

9. A circuit according to claim 8, wherein the amplifier of the control means comprises a comparator and, in use, the control transistor of the control means causes said one of the subsidiary main current carrying sections to be turned off.

15

10. A circuit according to claim 8, wherein the amplifier of the control means comprises an operational amplifier and, in use, the control transistor of the control means causes the current flowing through said one of the subsidiary main current carrying sections to be reduced gradually.

20

11. A circuit according to any one of the preceding claims, wherein the power semiconductor switch comprises a field effect device having a plurality of active cells sharing a common region coupled to the first main electrode with the main and sense current carrying sections having different numbers of active cells and the ratio between the number of active cells in the main and sense current carrying sections determining the ratio between the current carrying capabilities of the main and sense current carrying sections.

25

12. A circuit according to claim 11, wherein the power semiconductor switch comprises a power MOSFET or IGBT.

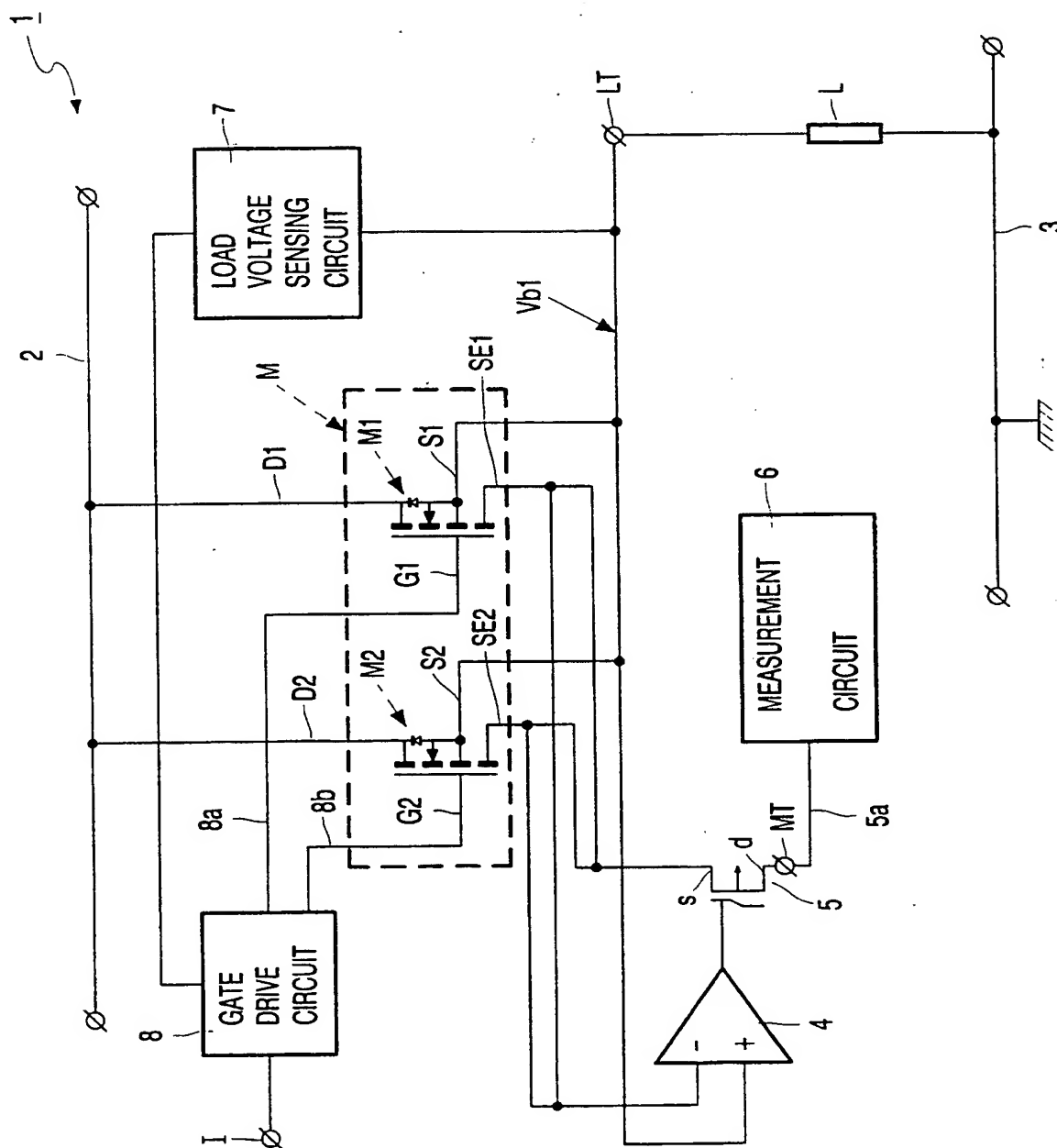
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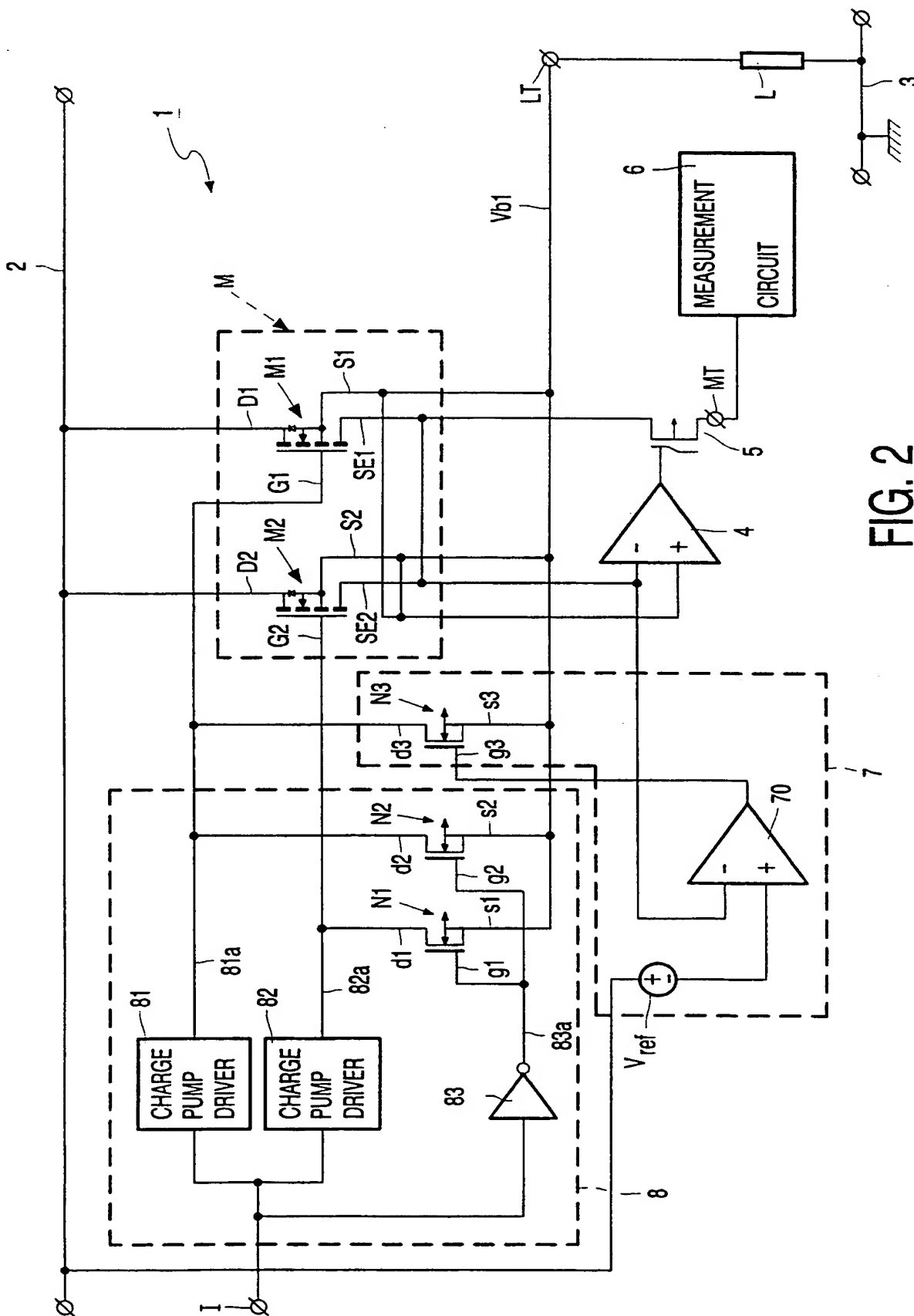
13. A circuit according to any one of the preceding claims in the form of an integrated circuit.

14. A power semiconductor device for use as the power  
5 semiconductor switch in a circuit in accordance with any one of the preceding claims, the device comprising a semiconductor body having first and second opposed major surfaces with a regular array of active cells formed in the body and separated from one another by a control gate structure at the first major surface, each active cell comprising a source region of one conductivity type  
10 separated from a region common to the active cells and of the same conductivity type as the source regions by a body region defining adjacent the control gate structure a conduction channel area controllable by the control gate structure, the common region being coupled to a first main electrode, the active cells comprising a plurality of groups of active cells and the control gate structure  
15 comprising a plurality of subsidiary control gate structures each associated with a respective different one of said groups and each coupled to a respective different one of a plurality of control electrodes, each group of active cells comprising a first set of active cells forming a main current carrying section and having their source regions coupled to a main current carrying electrode on the first major  
20 surface and a second smaller set of active cells forming a sense current carrying section and having their source regions coupled to a sense current carrying electrode on the first major surface.

15. A device according to claim 14, wherein the control gate structure  
25 is provided in a trench extending into the semiconductor body from the first major surface.

FIG. 1





**FIG. 2**



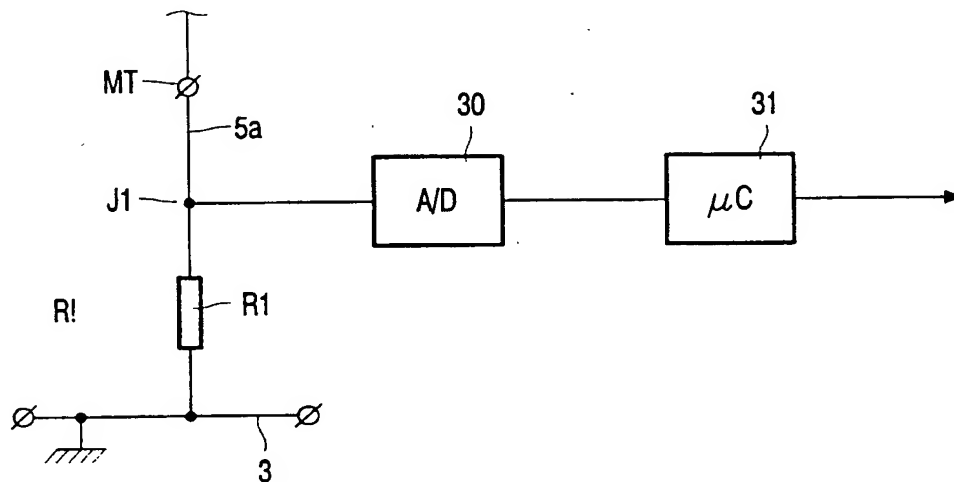


FIG. 3

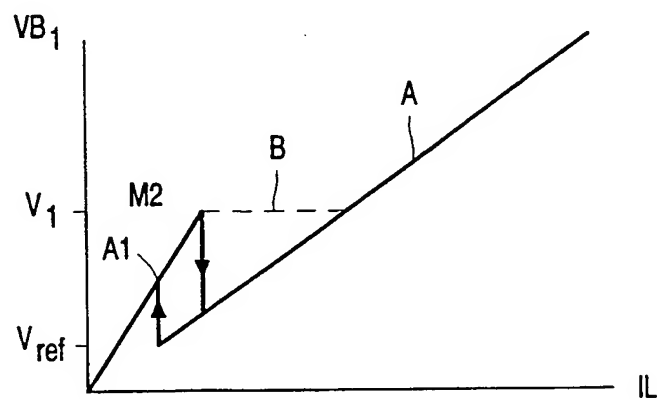


FIG. 4

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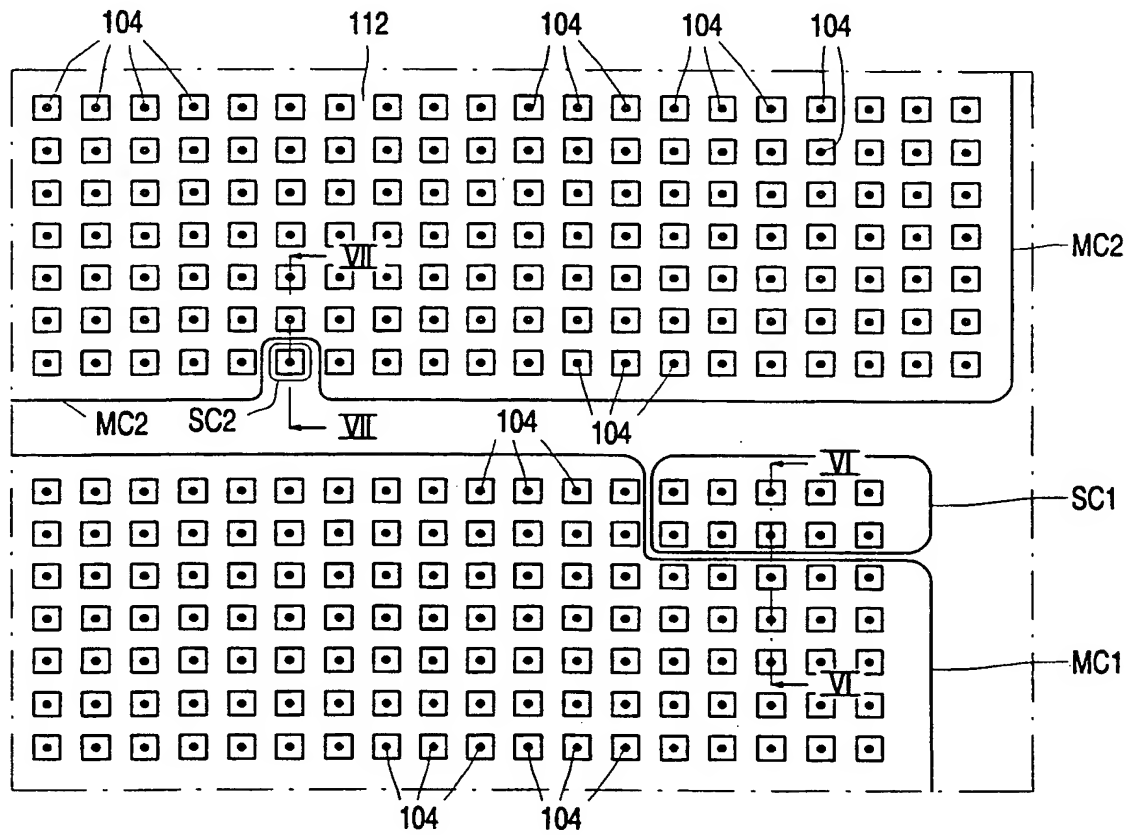


FIG. 5

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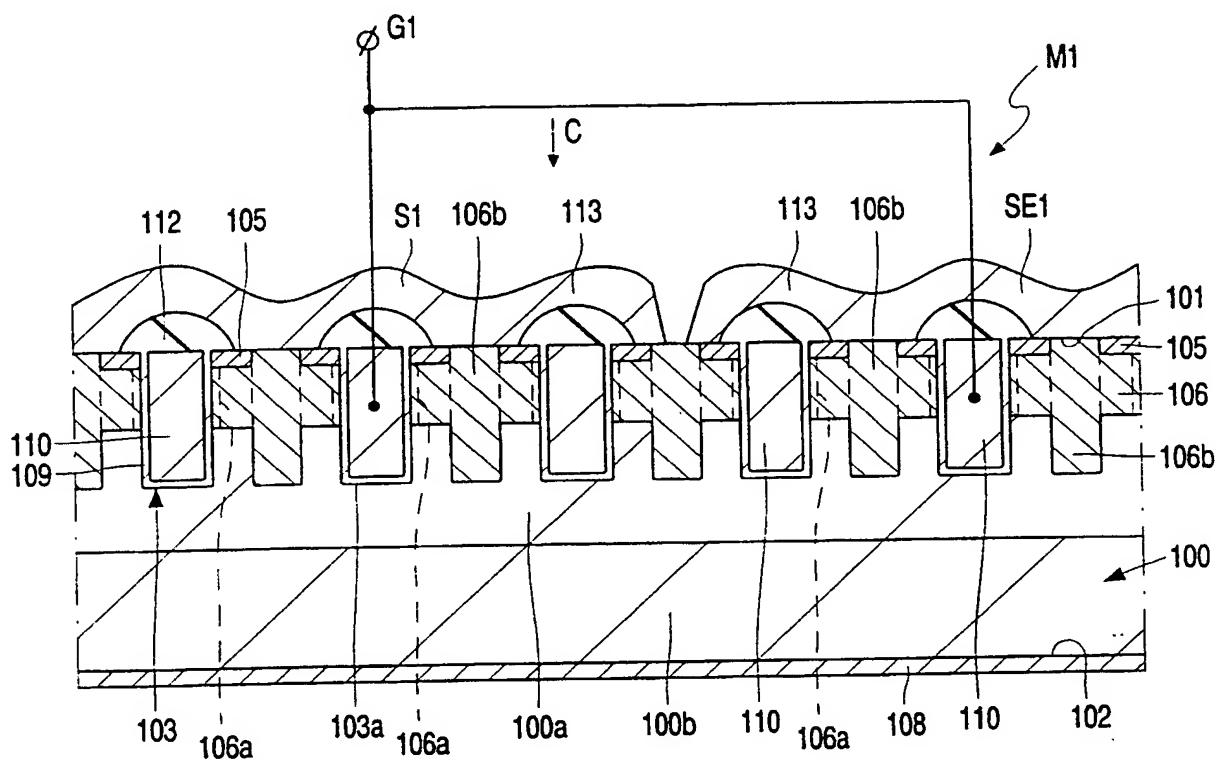


FIG. 6

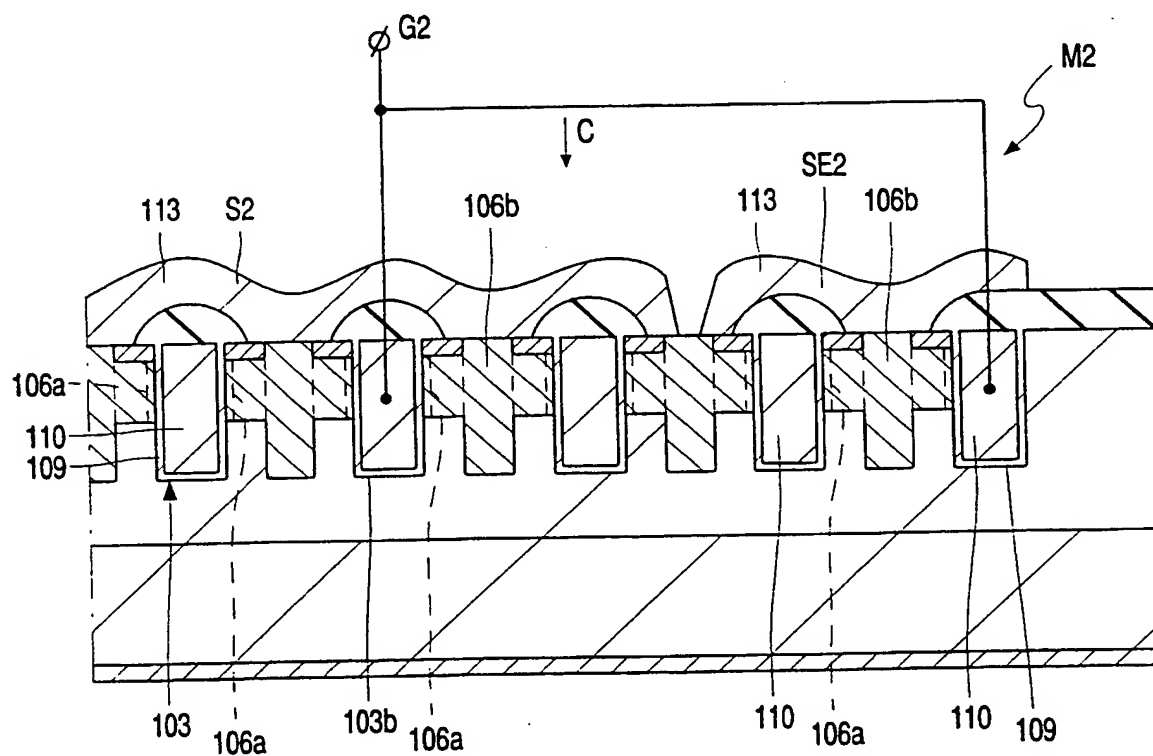


FIG. 7

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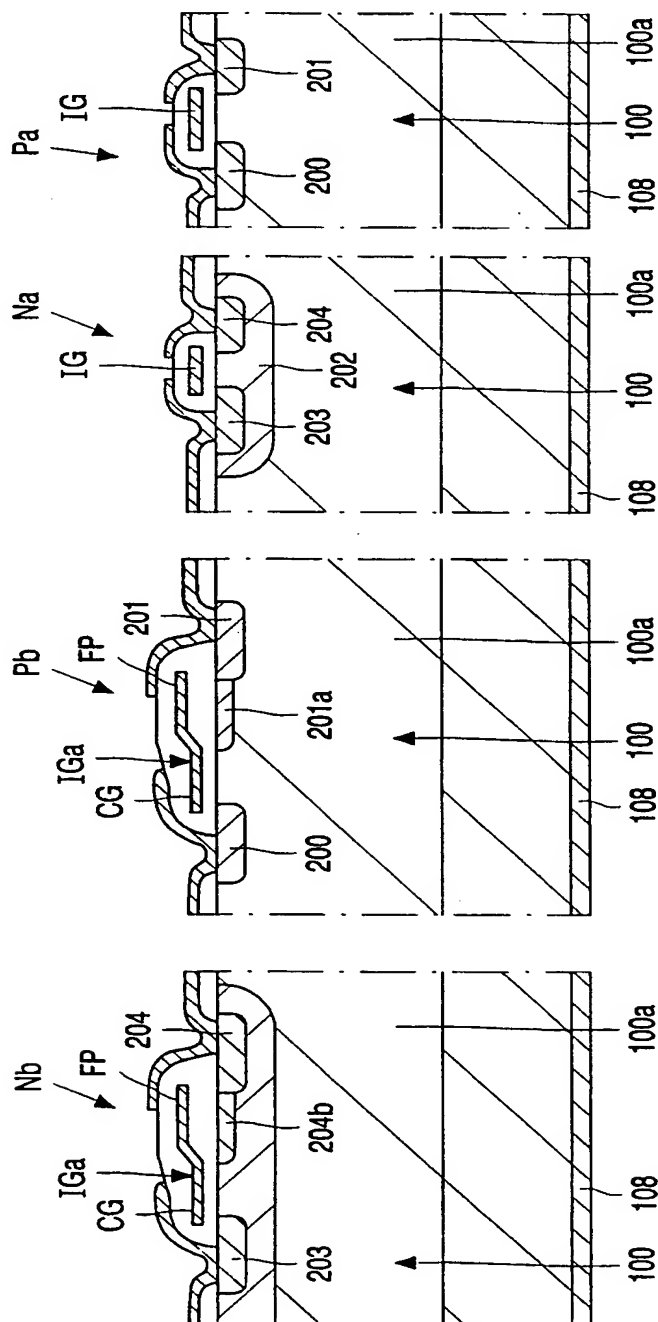


FIG. 8

## INTERNATIONAL SEARCH REPORT

Int. Application No

PCT/EP 00/03045

## A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 H03K17/12 H03K17/082

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H03K G05F G01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

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A	WO 97 45957 A (HITACHI LTD ; IJIMA TETSUO (JP); YANOKURA EIJI (JP); FUJIKI ATSUSH) 4 December 1997 (1997-12-04) abstract; figures 2,7	1,2
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Further documents are listed in the continuation of box C.



Patent family members are listed in annex.

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Date of the actual completion of the international search

7 August 2000

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## C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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